We claim:

1. A circuit comprising an input terminal for connection to a voltage source having first and second levels and a transition between the levels, a driver including first and second opposite conductivity type transistors, each including a control electrode and a path switched on and off in response to a voltage applied to the control electrode being on opposite sides of a threshold, the first and second transistor paths being connected in series across opposite power supply terminals, an output terminal between the paths, circuitry connected between the first terminal and the control electrodes for causing the first and second transistor paths to be respectively (a) on and off while the voltage source has the first level and (b) off and on while the voltage source has the second level, and at least one switched capacitor connected between the first terminal and the driver for preventing the paths of the first and second transistors from being on simultaneously during transitions between the first and second levels.

2. The circuit of claim 1 wherein the at least one switched capacitor is switched between a finite capacitance value and a substantially open circuit in response to the voltage across the at least one switched capacitor changing between opposite sides of a threshold voltage between the first and second levels.

3. The circuit of claim 2 wherein the at least one switched capacitor is connected in shunt with at least one of the control electrodes.

4. The circuit of claim 3 further including a resistive impedance connected to supply current to the shunt capacitor in response to the voltage at the input terminal.

5. The circuit of claim 4 wherein said first and second transistors are respectively a PFET and an NFET and said at least one capacitor comprises a field effect transistor.

6. The circuit of claim 5 wherein said resistive impedance, PFET, NFET and said at least one capacitor are included on an integrated circuit chip, and said resistive impedance comprises a resistor.

7. The circuit of claim 2 wherein said first and second transistors are respectively a PFET and an NFET and said at least one capacitor comprises a field effect transistor.

8. The circuit of claim 1 wherein the at least one capacitor includes first and second voltage controlled switched capacitors respectively connected to delay coupling of the transitions to the control electrodes of the first and second transistors.

9. The circuit of claim 8 wherein said first and second capacitors are respectively connected in shunt with the control electrodes of the first and second transistors and are such that (a) the first capacitor has a finite capacitance value on a first side of a first voltage threshold and is substantially an open circuit on a second side of the first threshold, and (b) the second capacitor has a finite capacitance value on a second side of a second voltage threshold and is

substantially an open circuit on a first side of the second threshold, the first and second thresholds differing from each other and being between the first and second levels.

10. The circuit of claim 9 wherein the first and second transistors are respectively a PFET and an NFET and the first and second shunt capacitors are respectively an NFET and a PFET.

11. The circuit of claim 9 further including first and second resistive impedances respectively connected to supply current to the first and second shunt capacitors in response to the voltage at the input terminal.

12. The circuit of claim 11 wherein the first and second transistors are respectively a PFET and an NFET and the first and second shunt capacitors are respectively an NFET and a PFET.

13. The circuit of claim 12 wherein the first and second transistors, the first and second resistive impedances, and the first and second shunt capacitors are included on an integrated circuit chip, the first and second resistive impedances including first and second resistors on the chip.

14. The circuit of claim 8 further including first and second inverters each having (a) an input terminal for enabling the first and second inverters to be simultaneously responsive to the voltage at the input terminal and (b) an output terminal, the output terminal of the first inverter being connected to supply current via a first DC path to the first shunt capacitor and the control electrode of the first

transistor, the output terminal of the second inverter being connected to supply current via a second DC path to the second shunt capacitor and the control electrode of the second transistor.

15. The circuit of claim 14 wherein the first and second transistors are field effect transistors, the first and second inverters comprise field effect transistors, and the first and second capacitors comprise field effect devices.

16. The circuit of claim 15 wherein all of the field effect transistors and devices are included on an integrated circuit chip including first and second resistors respectively connected in circuit with the first and second field effect transistors and the first and second inverters.

17. The circuit of claim 16 wherein the first and second resistors are respectively included in the first and second inverters.

18. The circuit of claim 17 wherein the first and second transistors are respectively a PFET and an NFET, each of the inverters including a PFET and an NFET, the PFET and NFET of each inverter having a source drain path and a gate electrode having a connection to the input terminal so that the gate electrodes of the PFETs and NFETs of the inverters are driven in parallel by the voltage at the input terminal, the output terminal of each of the inverters being between the source drain paths of the PFET and NFET thereof.

19. The circuit of claim 18 wherein the first resistor is connected between the source drain path of the NFET of the first inverter and the output

terminal of the first inverter, the second resistor being connected between the source drain path of the PFET of the second inverter and the output terminal of the second inverter.

20. The circuit of claim 19 wherein the first and second capacitors respectively include an NFET and a PFET.

21. The circuit of claim 20 wherein the NFET and PFET included in the first and second capacitors respectively have different first and second thresholds between the first and second levels, the NFET included in the first capacitor having a finite capacitance value for voltages below the first threshold and being a substantially open circuit for voltages greater than the first threshold, the PFET included in the second capacitor having a finite capacitance value for voltages greater than the second threshold and being a substantially open circuit for voltages less than the second threshold, the first threshold being greater than the second threshold.

22. A method of operating a driver including first and second opposite conductivity type transistors, each including a control electrode and a path between a pair of further electrodes controlled in response to a voltage applied to the control electrode, the paths of the first and second transistors being connected in series across opposite power supply terminals, an output terminal between the series connected paths, first and second switched capacitors respectively connected in shunt with the control electrodes, the method comprising: during a first interval: turning on and off the paths of the first and second transistors, respectively, while the second capacitor is charged and the

first capacitor is switched off by applying (a) a first voltage having a first value to the control electrode of the first transistor, (b) the first voltage value across the second capacitor, and (c) a second voltage having the first value to the control electrode of the second transistor; during a second interval: turning off and on the paths of the first and second transistors, respectively, while the second capacitor is switched off and the first capacitor is charged by applying (a) the second value of the first voltage to the control electrode of the first transistor, (b) the first voltage value across the first capacitor, and (c) the second value of the second voltage to the control electrode of the second transistor; during an initial portion of a first transitional period between the first and second intervals: turning off the path of the first transistor while maintaining the path of the second transistor off by changing the first voltage from the first value toward the second value while the first capacitor remains turned off and the second capacitor is charged; during a second portion of the first transitional period turning on the path of the second transistor while maintaining the path of the first transistor off by changing the charge on the second capacitor so that there is a change in the value of the second voltage from the first value toward the second value; during an initial portion of a second transitional period between the second and first intervals: turning off the path of the second transistor while maintaining the path of the first transistor off by changing the second voltage from the second value toward the first value while the second capacitor remains turned off and the first capacitor is charged; and during a second portion of the second transitional period turning on the path of the first transistor while maintaining the path of the

second transistor off by changing the charge on the first capacitor so that there is a change in the value of the first voltage from the second value toward the first value.

23. The method of claim 22 further comprising the steps of: switching off the first capacitor during the second portion of the first transitional period prior to the value of the first voltage, as applied to the control electrode of the first transistor, reaching the first value; and switching off the second capacitor during the second portion of the second transitional period prior to the value of the second voltage, as applied to the control electrode of the first transistor, reaching the second value.

24. The method of claim 23 wherein the first and second capacitors are switched on and off in response to the first and second voltages having values on opposite sides of first and second thresholds respectively associated with the first and second capacitors.